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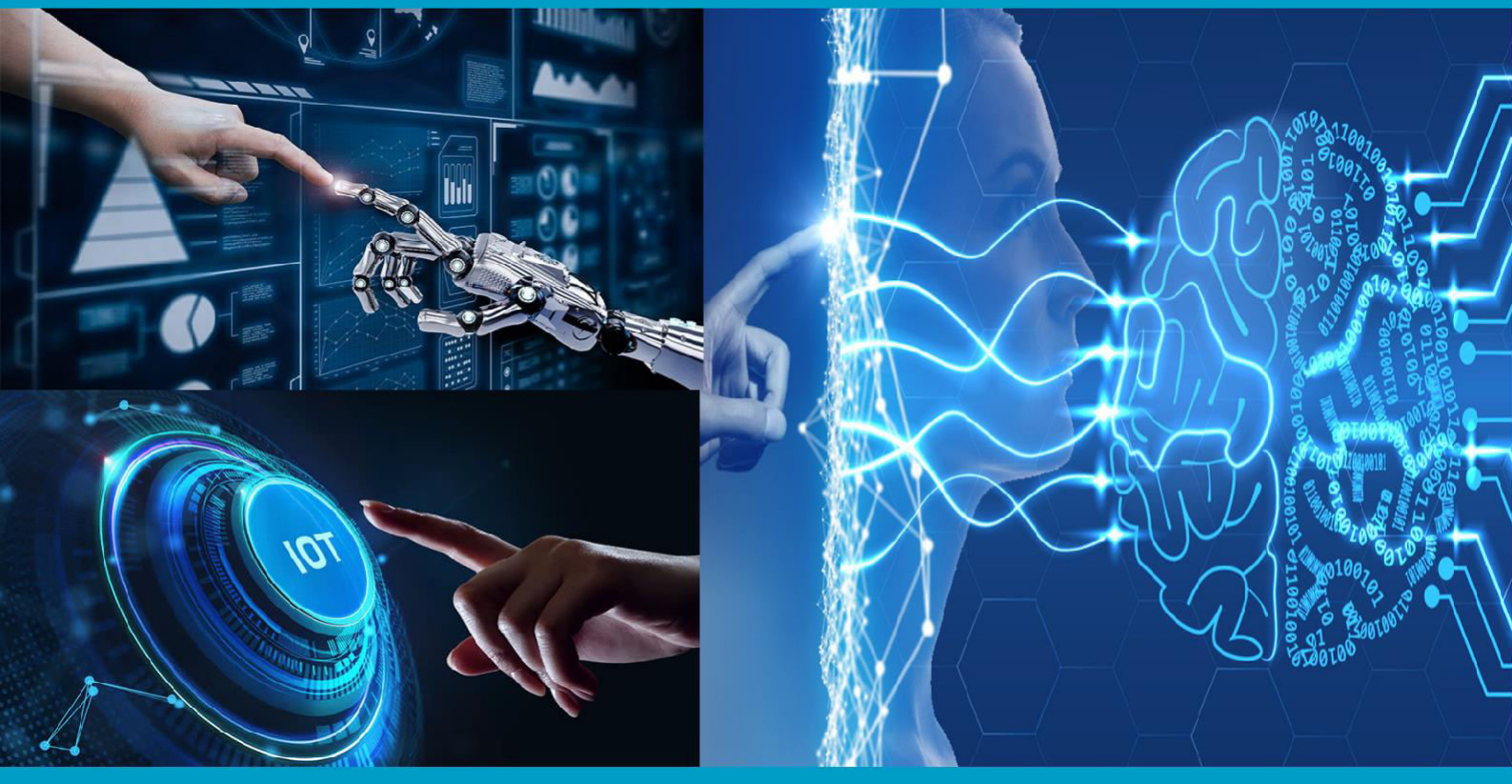

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Sorting Network Generated Quick Binary Counters and Compressors

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ABSTRACT: The critical path in various digital signal processing devices includes the parallel summing of several operands. High compression ratio is used to speed up the summing. Compressors and counters are required. In this article, we offer a brand-new sorting network-based technique for fast saturated binary counters and exact/approximate(4:2) compressors. In order to create reordered sequences that can only be represented by one-hotcode sequences ,the inputs of the counter are a symmetrically split into two groups and fed into sorting networks. Three unique Boolean equations are constructed between the reordered sequence and the one-hot code sequence, which can greatly simplify the output Boolean expression soft he counter. We build and further refine the(7,3) counter using the aforementioned technique, which can perform27.0% 26.2%,

KEYWORDS: Sorting network,one-hot code,multiplier,exact/approximate 4:2 compressor,binary counter

I. INTRODUCTION

The critical path includes the summation of several operands, which is frequently utilizedin different digital signal processing (DSP) units. The Wallace Tree structure [1], whose performance is the basic multiplier's bottleneck, is used in a basic multiplier circuit to add upall the partial products. Big number multipliers based on Toom-Cook [4] or the Kasturbamethods [3] are used by public-key crypto systems like RSA and Elliptic Curve Crypto graphy (ECC) to create modular multipliers. These two methods have been the subject of several studies and hardware implementations. Many circuit components in these works, like in [5],make use of the summation of numerous operands. In order to provide high security in cloud computing, fully homo morphic encryption (FHE), a post-quantum cryptosystem, urgently requires Number Theoretic implementations, the total of several operand smakes up the central processing unit. Wallace Tree structure [1] and its modified method Reduced WallaceTree [2] are the most well-known multiple operands summation techniques. These technique shave logarithmic time consumption because they speed up the summing by using full addersas (3, 2) counters. Carry save structures are another name for this kind of building. Since then,other works, including [7], [8], [9], [10], [11], [12], have examined how to build a more time-efficient framework to speed up the summing. The fundamental idea is to consider more bitswith the sameweight in orderto build acounteror compressor with alargercompressionratio than the (3, 2) counter. For instance, the structure of a basic (7, 3) counter with full adders is depicted in Fig. 1.

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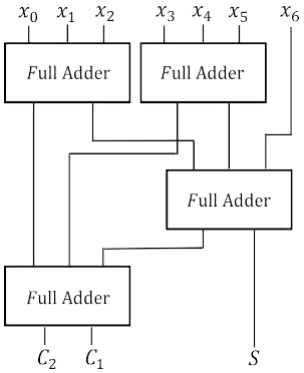

Fig1:(7,3)counter combined by counter

II. REVIEW OF SORTING NETWORK

An effective parallel hardware network used for data sorting is the sorting network [14]. According to the well-known0, 1 principle [14], and any type of number can be sorted if asorting network can sort a batch of data whose constituents are all 1-bit numbers. We only use it for1-bit data sorting in this paper.

A. Sorting Network Working Principle

Fig. 2 displays the conventional three- and four-way sorting networks [14]. With two datainputs and two data outputs, and only 1 bit numbers, each vertical line represents a sorter.Always, the sorter places the larger input higher and the smaller input lower. We provide aninput example in Fig. 2: The four-way sorting's input is represented by the sequence [0, 1, 1,and1].

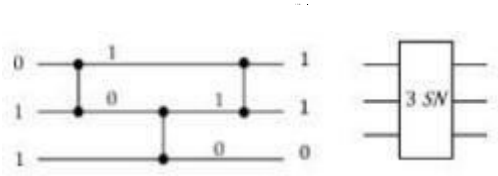

Fig2: Three-andfour-waysortingnetworks

B. SORTERFOR 1BITDATA

The sorter reorders two inputs according to numerical magnitudes, as was alreadyindicated. The logical circuit shown in Fig. 3 can easily sort two 1-bit pieces of data. As aresult, a sorter uses one layer of basic logic gates with two inputs, where as three- and four-way sorting networks each use three layer softhese gates.

III. EXISTING WORK

In this step, we build a useful counter (7, 3). We quickly review the design in [11]to serve as the primary comparison n object. An extremely quick (6, 3) counter with a symmetric stacking structure was proposed by Fritz and Fam [11], and they built a (7, 3) saturated counter from this counter. Although it is the fastest relative to other (7, 3) counter designs, its delay performance is lower because there was no optimization done before a MUX was simply added to the critical path. We suggest using this technique to directly generate a (7, 3)counter to address the issue in [11].Un like the symmetric stacking structure, we begin with two asymmetric sorting networks,as shown in Fig.2. We build three unique Boolean equations through the creation of one-hot code sequences.

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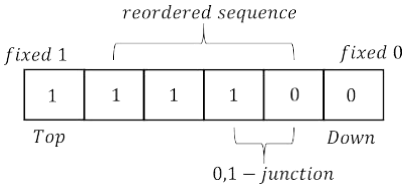

Fig3: Definition of a sequence

If there are any "1"s, they are all at the bottom of the sequence, and vice versa. There must be a location in the reordered sequence where the junction of "1" and "0" is if there are both"1s"and"0s,"respectively.

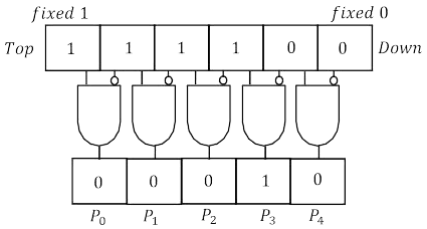

Fig4: One hotcode generation

If there are only "1"s or "0"s, we can control the sequence by padding the reordered sequencewith a fixed bit "1" at the top and a fixed bit "0" at the bottom to ensure that the 0,1-junctionalways exits. Second, the total number of "1"s and "0"s in the rearranged sequence is the sameas it was in the initial sequence (the inputs of two sorting networks). The padded "1" is fixed; therefore even though it would have an impact on the overall number of "1s" in the padded sequence, weignore it.

C. One-hotcodegeneration

A symmetric Pre-recorded: As shown in Fig. 2, three layers of binary sorters are needed for both three- and four-way sorting networks (the two binary sorters on the same layer in four-way sorting network can be calculated in parallel). As depicted in Fig. 3, one fundamental two-input logical gate layer is consumed by each layer of binary sorters. This means that the three-and four-way sorting network stake approximately the same amount of time.We then divide the seven inputs of a (7, 3) counter into two groups based on this. Where as the othe rcomponent only has three bits, the first part has four.

1) Find the one-hotcode sequence and the 0,1-Junction:As seen in Fig. 4, the promise ofthe extended fixed "0" and "1" allows the 0,1-junction to only reflect the reorderedsequence. Keep in mind that the 0, 1-junction must be located 1,0 from left to right. As aresult, we continue to use the four-way sorting network as an example, followed by the structure shown in Fig. 5.

2) With the use of the Boolean expression (AB), this structure creates the new sequences P0-P4.There is only one"1"in the sequence P0-P4 since there is only one0, 1-junction in there arranged and expanded sequence.

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III. RESULTS

I .VIEWINGANDSIMULATINGTHEOUTPUTWAVEFORMS

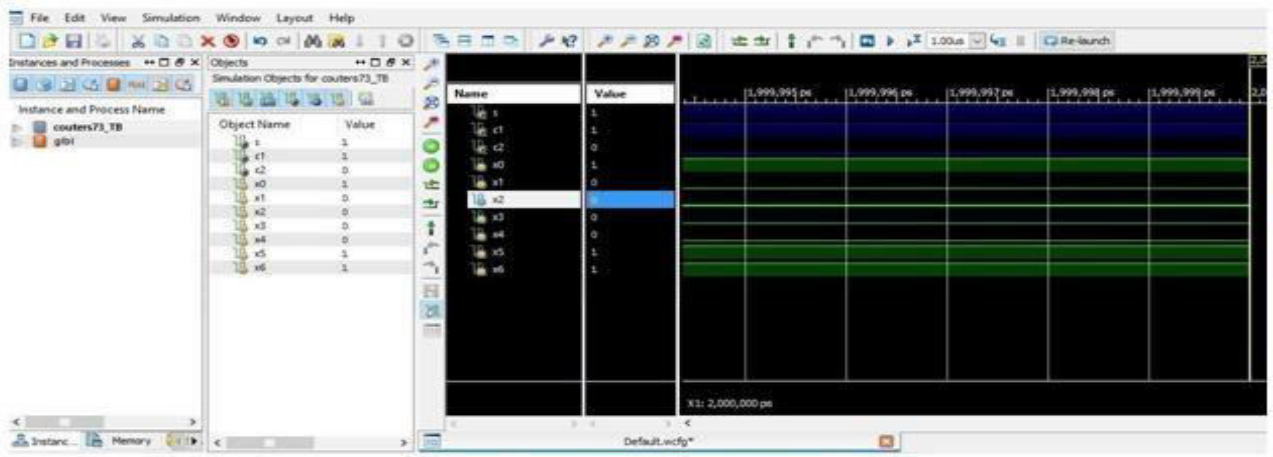

Fig7: Output Wave formsfor (7,3)counter

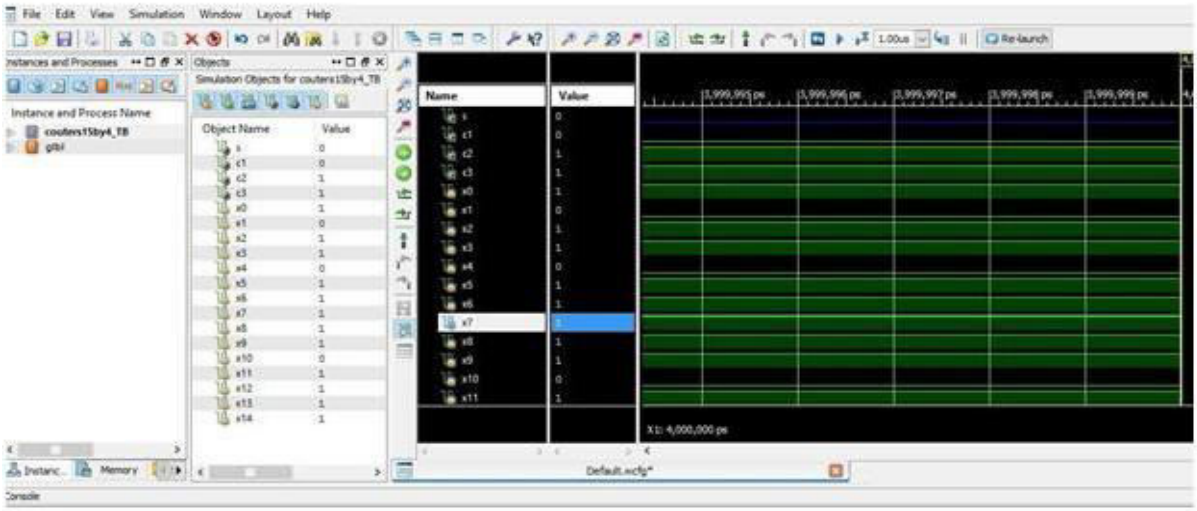

Fig8: Output Waveformsfor(15,4) counter

II SYNTHESIS AND IMPLEMENTATION OF THE DESIGN

About Execution, click to use synthe size-XST, double click on the chosen existing file. If there are any errors fix them.Click on there ports and the design overview.

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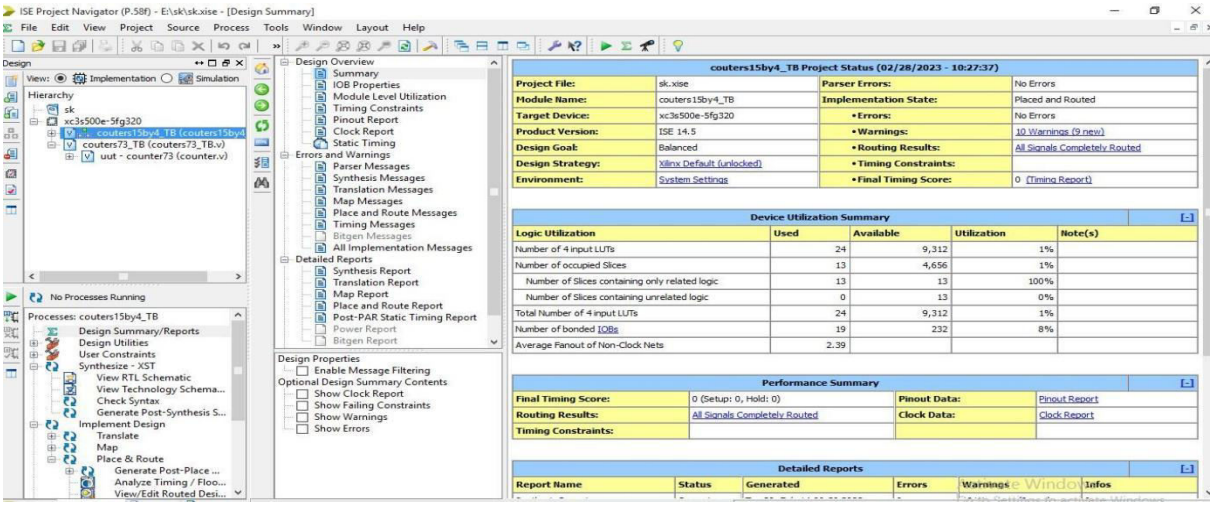

Fig9: Design Synthesis

III. *VIEW RTL SCHEMATIC*

When synthesize-XST isex panded, select see RTL Schematic and then click OK.

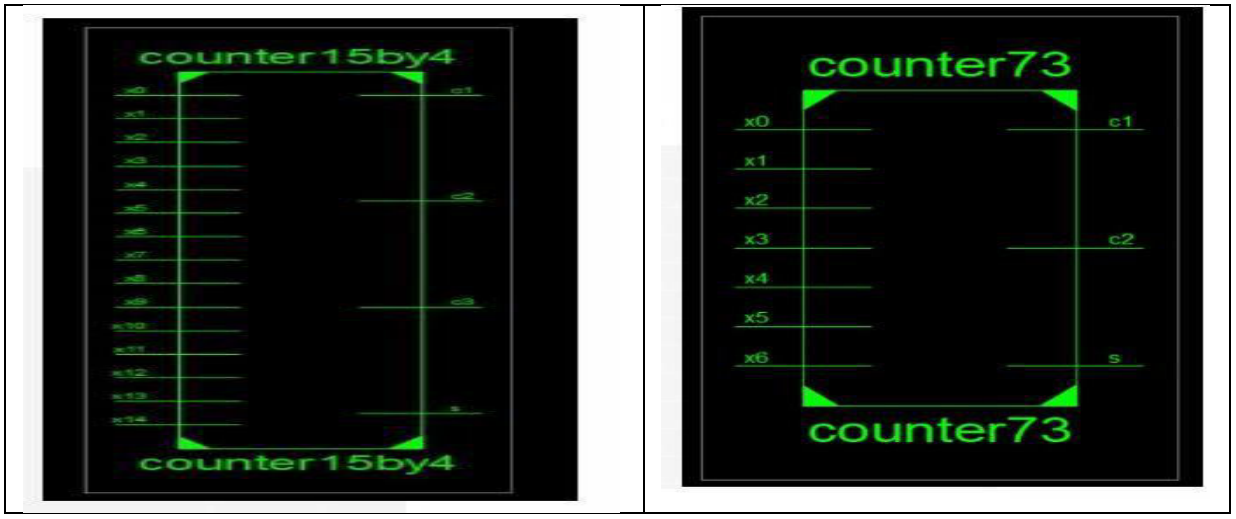

Fig10(a)RTLSchematicfor(15,4)counter(b)**:**RTLSchematicfor(7,3)counter

IV. CONCLUSION

This paper plans and replicates a strategy for a swift and effective counter attack. A double counter with reference to a unique symmetric piece .The proposed calculation method uses aggregate and convey. Throughout this procedure, a brand-new counter design technique based on a sorting network is put forth. Because proposed counters accomplish less latency where speed is a factor and out perform previous designs in ADP,they are more adaptable than present designs.

REFERENCES

[1] Modified Booth multipliers with a regular partial product array: Shiann-RongKuang,Jiun-Ping Wang, and Cang-Yuan Guo, IEEE Trans. on Circuit and Systems, vol. 56, no. 5, p.404–408,May2009.

[2] A well-structured modified Booth multiplier design by Li-rong Wang, Shyh-JyeJou, andChung-LenLeewaspublishedintheProc.ofIEEEVLSI-DATinApril2008,pp.85-88.

[3] A 320-MHz 8bit x 8bit pipelined multiplier at ultra-low supply voltage was described byYung-chin Liang, Ching-ji Huang, and Wei-bin Yang in Proc. of IEEE A-SSCC, pp. 73-76, inNovember 2008.

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