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Enhanced Capacitance Multiplier in 180nm Technology

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ABSTRACT: A current-mode capacitor multiplier using a differential amplifier with exponential current scaling is presented. The proposed circuit consists of a reduced implementation of a multiplier based on differential amplifiers with decreased need for parameter matching compared with a conventional structure, thus reducing the power consumption and silicon area. It includes an exponential current scaling scheme to provide a large multiplication factor. Additionally, the differential input stage offers the capability to implement a floating realization for bidirectional applications. Experimental results from a fabricated prototype in 0.18-μm technology show the operation of the floating realization.

KEYWORDS: Analog integrated circuits, capacitor multiplier, low-voltage analog circuits.

I. INTRODUCTION

The implementation of high valued Capacitors in integrated silicon circuits is limited by the chip area that they occupy. To face this limitation, there is a good alternative i.e. to implement an active circuit that emulates a capacitance several times larger than that of the physical capacitor. For example, the Miller effect capacitor multiplier (voltage-mode approach) uses an inverting voltage amplifier connected across the terminals of a capacitor. As a result, the equivalent capacitance obtained is $(1+A_v)C_{ph}$, where C_{ph} is the physical capacitor and A_v is the gain of the amplifier . However, this scheme has serious swing limitations since the maximum voltage applied to the capacitance is reduced by the scaling factor.

The another type of multipliers, i.e., current-mode multipliers, is based on magnifying the capacitive effect by means of current scaling. Fig. 1(a) shows the concept of operation, where a current in a capacitor C, i.e., i_c, is sensed; a current controlled current source multiplied by a factor k sinks the magnitude ki_c, which results in an output current $i_o = i_c(1 + k)$, thus exhibiting an equivalent capacitance of $C_{eq} = C(1 + k)$.

Conventional topologies straight forward based on this scheme offer good accuracy but exhibit limited multiplication factor, decreased effective bandwidth, and increased power and silicon area and only allow single-ended implementation [3]–[5].

In this paper, a reduced topology based on a differential amplifier is proposed, which offers the implementation of a floating realization for analog applications.

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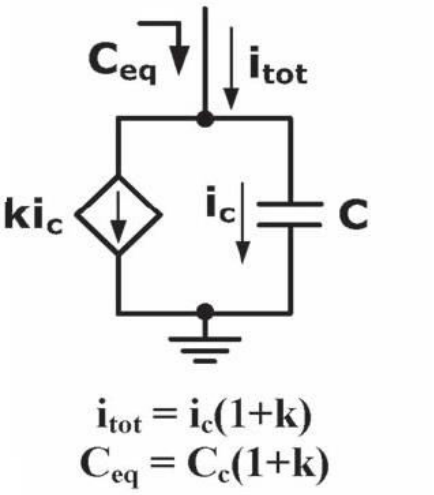

Fig 1 Concept of operation of Current mode Capacitance Multiplier

II. RELATED WORK

The proposed circuit is shown in Fig. 2. It consists of a single differential pair formed by transistors M1–M6. Additionally, there is a multiplier section which multiplies the current value at the output of differential stage thus offering the factor *k* with the advantage of including a differential input stage. This increases the multiplication factor exponentially to k=1+k1k2k3 with reduced silicon area and power consumption. For the same scaling factor k and assuming equal gain factors of $k_1 = k_2 = k_3 = k_x$, the proposed circuit has an addition in power consumption and silicon area proportional to the factor $3(k_x + 1)$.

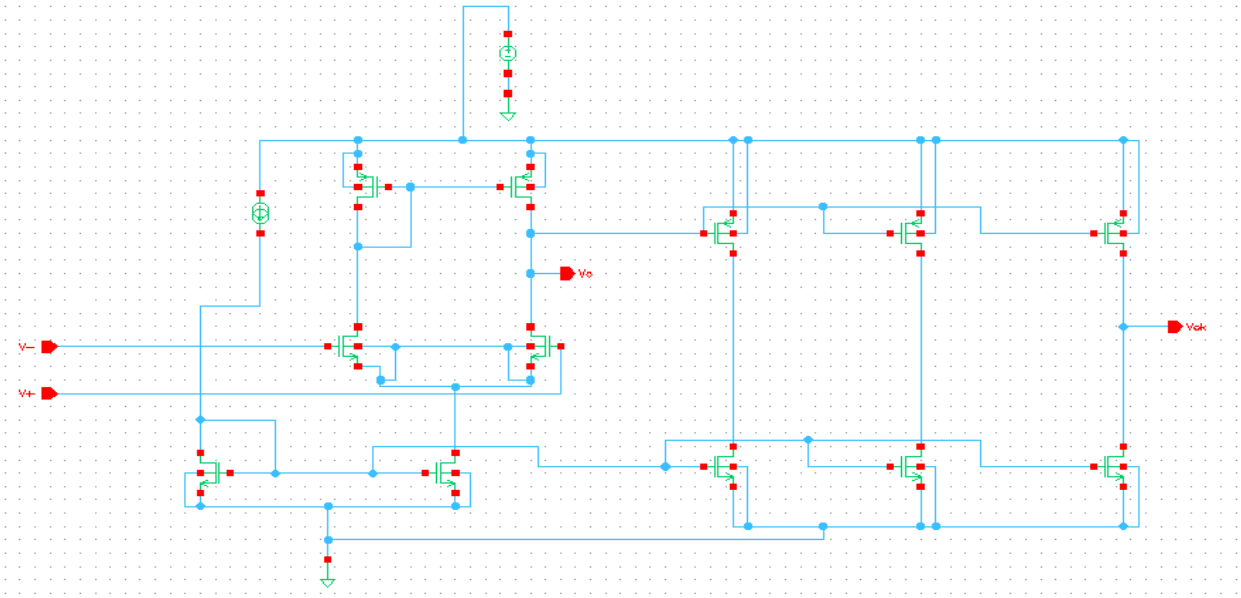

Fig. 2 Proposed Capacitance Multiplier Circuit

The differential input stage offers an important advantage. It has the ability to define a voltage at both input terminals; if the non inverting input of the implementation is connected to ground, it operates as a grounded capacitor. However,

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this input can be utilized to sense other voltage variations; thus, an additional terminal may be defined in order to operate the circuit as a floating capacitor. The W/L ratio of transistors used in the proposed circuit is given below in Table 1.

Transistor Names	W/L Ratio(μm/μm)
M1	1/0.18
M2	1/0.18
M3	1/0.18
M4	1/0.18
M5	1/0.18
M6	1/0.18
M7	3/1
M8	1/0.18
M9	9/3
M10	3/1
M11	27/9
M12	9/3

III. EXPERIMENTAL RESULTS

The open loop operation of the circuit is tested by giving inputs 0.85V DC, 1mV AC and 0.8V DC, -1mV AC at inverting and non inverting terminals respectively. The gain of Differential Amplifier is coming out to be ~45dB. The output current value of Differential Stage is I_o = 27.11μA and that of the Current Multiplier Stage is I_{ok} = 760.02μA. These output current values are in agreement with the desired multiplication factor of current i.e. 27. The supply voltage of V_{dd} = 1.8 V and a biasing current of I_b = 30μA. The open loop frequency response of the Capacitance Multiplier Circuit is shown in figure 3.

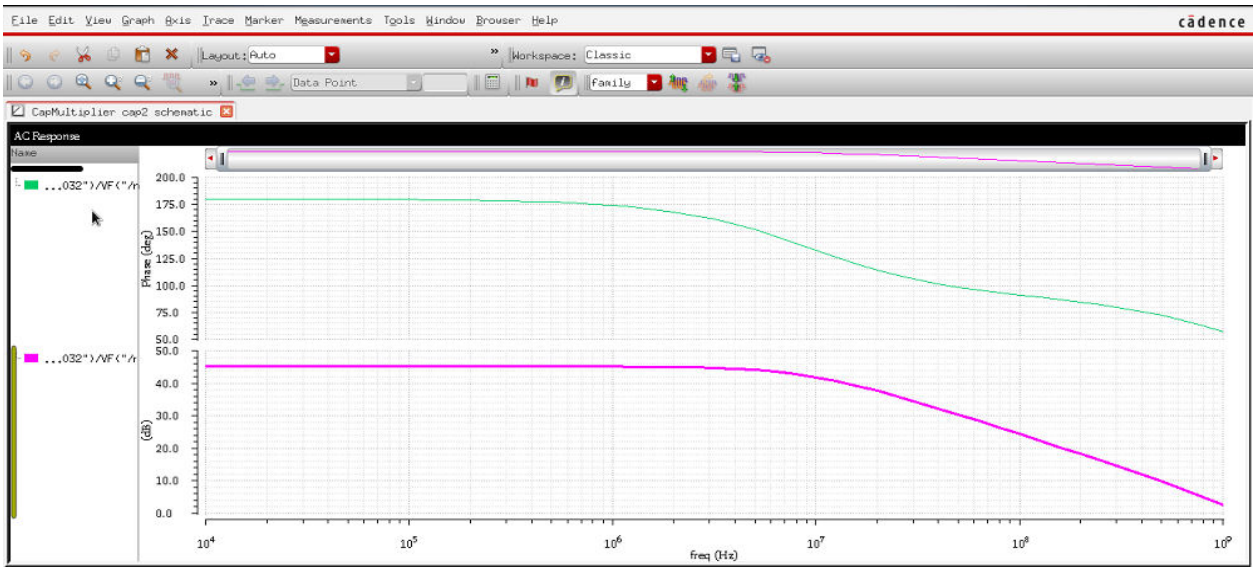

Fig. 3 Open loop frequency response of the proposed circuit

The value of K is chosen to be 28 which means that each substage of current multiplier stage is multiplying the current value by 3. The output current value of current multiplier stage is I_{ok}=760.02μA, which is k_1*k_2*k_3 times the I_o current i.e. 27 times the I_o current.

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The circuit is tested for capacitance multiplication by implementing it in a RC low pass filter using floating configuration. The value of base capacitance taken is 80 pF, resulting in an equivalent capacitance C_{eq} = 2.24 nF (including a parasitic capacitance of ~50 pF) combined with a resistor R = 22 kΩ. The measured cutoff frequency is ~ 3.1 kHz for floating implementation. The reduced value of -3dB frequency to 1/28 times from the one which should be 94.98 KHz for R= 22K and C= 80pF proves that Capacitance Value is multiplied 28 times. The power consumption of the circuit is reduced to 0.612mW. The Layout diagram of the proposed circuit is shown in Fig. 6. The Table 1 is showing the comparison of the results obtained from the proposed circuit with the previous works done so far.

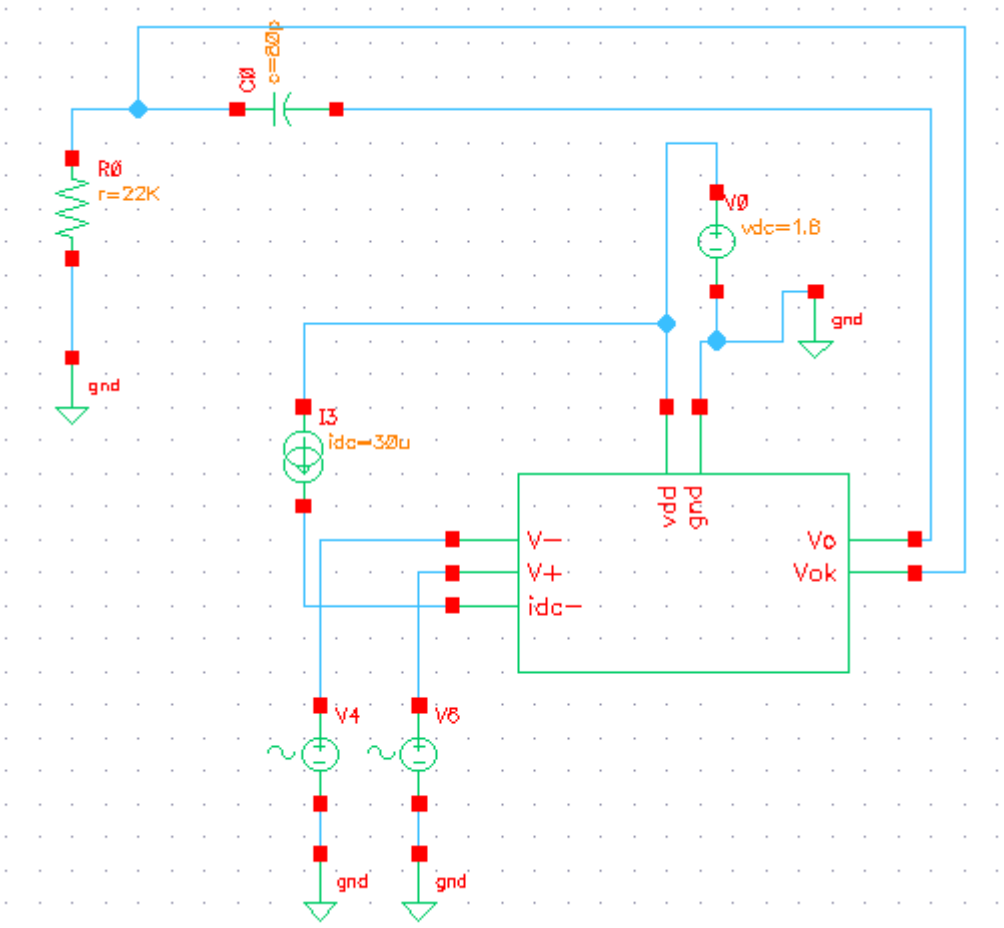

Fig. 4 Capacitance Multiplier Circuit implemented in a RC Low Pass Filter with Floating Implementation.

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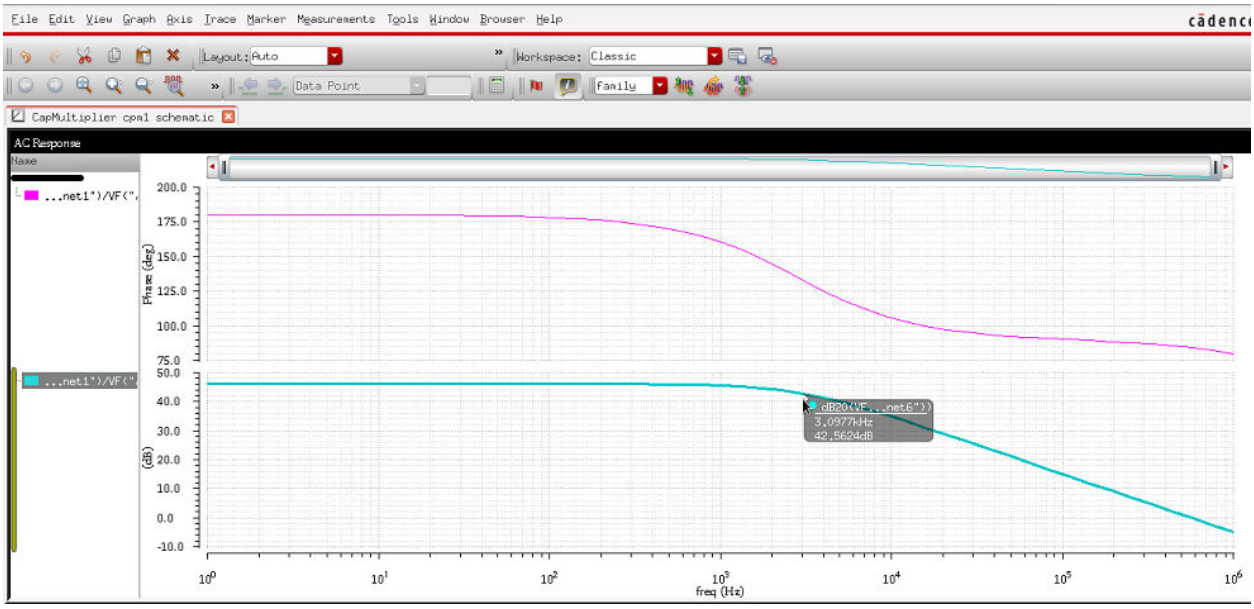

Fig. 5 Frequency Response of RC Low Pass Filter implemented by Capacitance Multiplier Circuit.

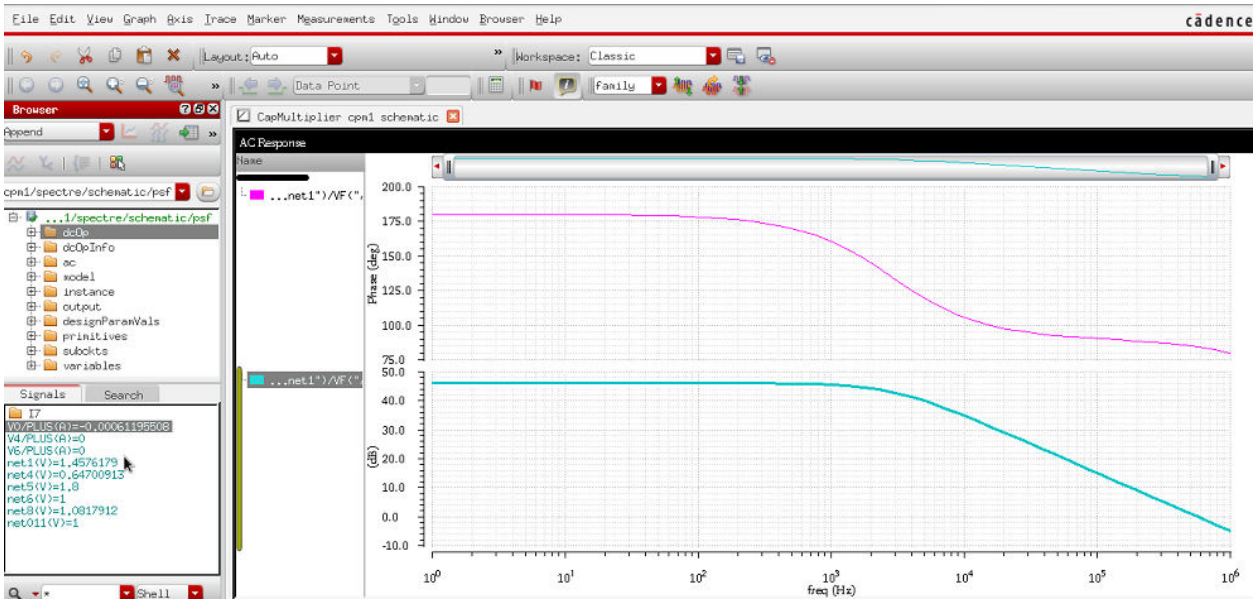

Fig. 6 Frequency Response of RC LPF showing Power Consumption in the Circuit.

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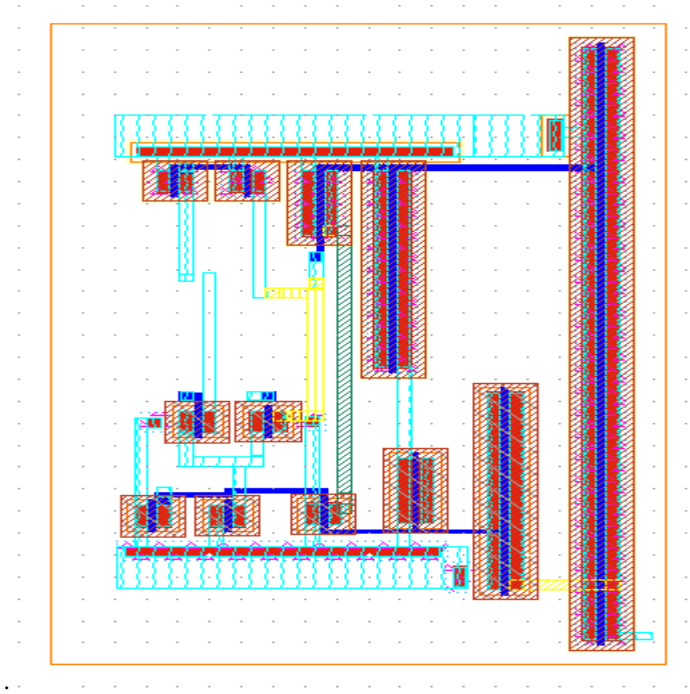

Fig. 7 Layout Diagram of proposed Capacitance Multiplier Circuit

Parameter	[3]	[4]	[5]	[9] (Base Paper Work)	Results Obtained
Technology (µm)	0.35	0.18	0.5	0.5	0.18
Multiplication factor	16	65	10.1	28	28
Base capacitance C (pF)	170	7.95	18	25	80
C_{eq} (pF)	2720	716	182	700	2240
Power Consumption (mW)	0.672	_	_	1.32	0.612
Min. Supply volt. (V)	_	_	_	1.3	1.8
Silicon area (mm^2)	_	_	0.0702	0.07	0.00056

Table 2 Comparison of measured parameters between Conventional Circuits and Proposed Circuit.

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IV. CONCLUSION

A capacitor multiplier based on a differential amplifier with exponential current scaling has been presented. The single differential input stage offering increased accuracy and reduced silicon area and power consumption was discussed. The differential input stage also offers the capability to implement grounded and floating realizations. Experimental results showing the operation of the floating circuit implemented in low-pass RC filter is presented.

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